III. Remarks

A. Rejection under 35 U.S.C. §102(e)

The Action rejects Claims 1-2, 6-7, 13-14, 17-19 and 21-22 as being anticipated by U.S. Patent Application Publication No. 2004/0051120A1 to Kato. Reconsideration of this rejection is respectfully requested in view of the following arguments.

Independent Claim 1 recites that the MOS device has a length and a width. The first and second source/drain regions of the device are spaced laterally apart relative to one another "along the length of said device." Claim 1 also recites that the dimension of the gate that is confined substantially within the active region of the device is substantially parallel to "the width of the device." It is submitted that Kato clearly does not teach a gate being configured such that a dimension of the gate, defined substantially parallel to the width of the device, is confined to be substantially within the active region of the device.

For purposes of better illustrating Applicants' arguments, the Examiner is directed to the attached Exhibit which includes an annotated copy of FIGS. 1(a) and 1(b) of Kato. Turning to the Exhibit, specifically to FIG. 1(b), source and drain regions 17 are shown formed in semiconductor layer 14. These regions are laterally spaced from one another along the length of the device and are formed in active region 14. Note that this designation of the "length" (L) direction of the device is conventional and is labeled in FIG. 1(b) and in FIG. 1(a). With the length of the device labeled in FIG. 1(a), Applicants have also labeled the width (W) direction in FIG. 1(a).

Turning now to the top view of Kato (FIG. 1(a)), gate 7 is shown formed having a small dimension in the length direction and a much larger dimension in the width direction. Active region 14 is also shown. From this illustration, it can be seen that the dimension of the gate that is defined substantially parallel to the width of the device (labeled "W" in FIG. 1(a)) is **not** confined to be substantially within the active region 14 of the device. Indeed, a very large portion of gate element 7, which Applicants circled and labeled "Extends beyond active region 14", is not confined to be substantially within the active region 14.

Still further, Claim 1 also recites that the device includes "an isolation structure formed in the semiconductor layer, the isolation structure being configured to substantially isolate one or more portions of the first source/drain region from corresponding portions of the second source/drain regions." Claim 1 makes clear that this isolation structure is formed to isolate source/drain regions **of the same device**, not of different devices. The Examiner relies on isolation structure 24 for providing this feature. However, with reference to FIG. 1(b), Kato clearly shows that isolation structures 24 are formed in between adjacent devices, not in between portions of the first and second source/drain regions of the same device. Indeed, Paragraph 49 of Kato cited by the Examiner expressly states that "[e]ach of the **element regions 14** can be in contact with the metallic layer 13, **while being separately insulated from one another** in a lateral direction by insulating layer 24." (emphasis added) It is noted that the top plan view of FIG. 1(a) does not even show regions 24, though it is submitted that it appears from the figures that isolation regions 24 will surround active regions 14 and not isolate portions of first and second source/drain regions 17 formed therein.

For at least these reasons, it is submitted that Claim 1 is not anticipated by Kato. Accordingly, it is submitted that Claim 1 and the claims which depend therefrom are allowable over Kato.

Independent Claims 14 and 21 also recite the gate and isolation structure features discussed above in connection with independent Claim 1. It is submitted, therefore, that for at least these reasons, Claims 14 and 21 are not anticipated by Kato and that these claims and the claims that depend therefrom are allowable over Kato.

Accordingly, reconsideration and withdrawal of the rejection of these claims are respectfully requested.

B. Rejection under 35 U.S.C. §103

The Action rejects Claims 3-5, 8-12, 15-16, 19-20 and 23 as being obvious from Kato in view of several other references. These claims depend from independent Claims 1, 14 and 21.

As set forth above, these claims are allowable for at least the reasons argued above for independent Claims 1, 14 and 21.

Reconsideration and withdrawal of the rejections of these claims are respectfully requested.

IV. Conclusion

In view of the foregoing remarks and amendments, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account 04-1679.

Respectfully submitted,

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EXHIBIT

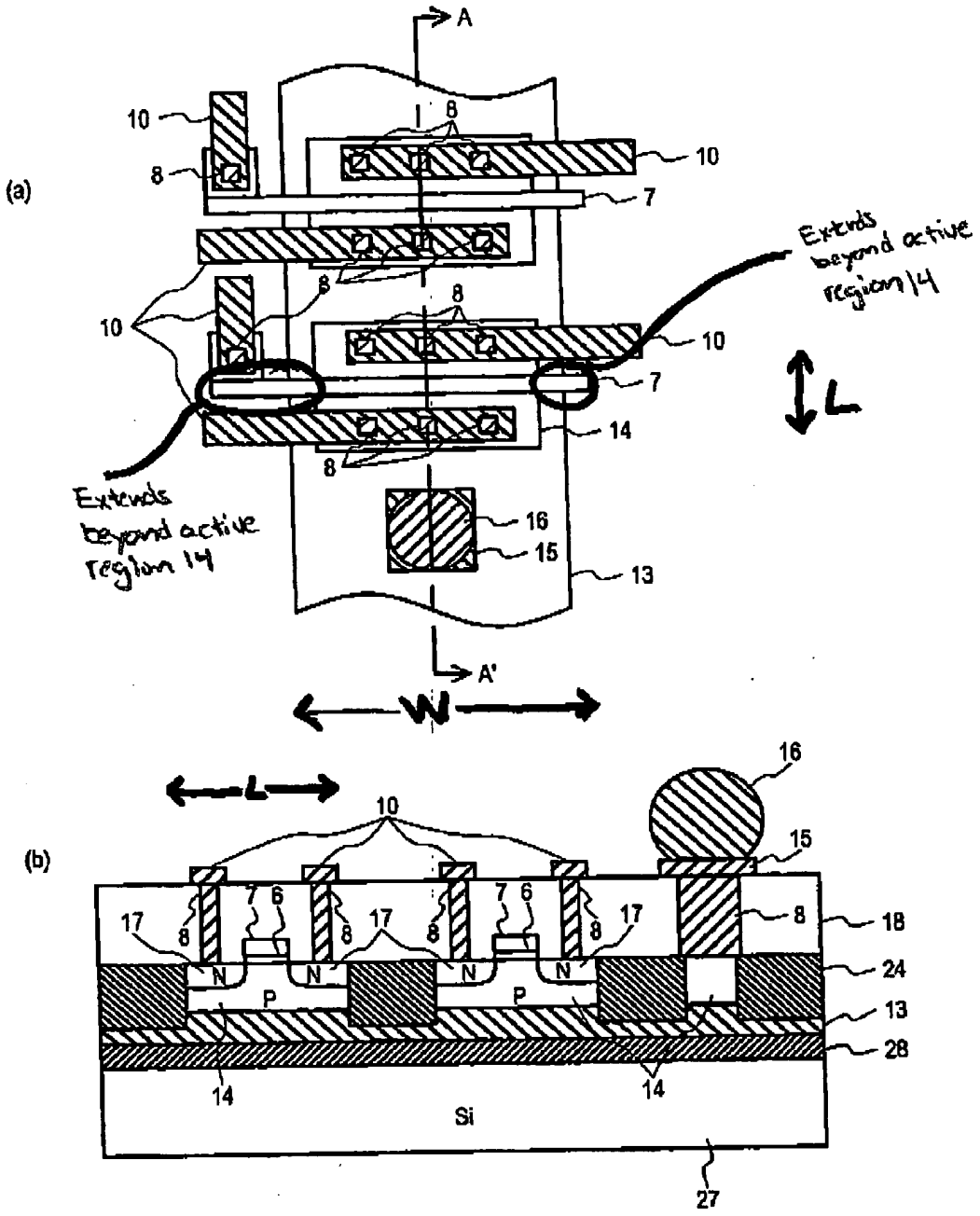
(a)
A
A'
W
L
10
8
7
14
16
15
13
Extends beyond active region 14
(b)
L
16
15
10
17
8
7
6
N
P
18
24
13
28
14
Si
27

FIG. 1